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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,133	03/26/2001	Hisao Suzuki	108075-00054	5889

7590 06/02/2004

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,133	SUZUKI ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43,47 and 48* is/are pending in the application.

4a) Of the above claim(s) *11-35* is/are withdrawn from consideration.

5)☒ Claim(s) *2-10* is/are allowed.

6)☒ Claim(s) *1,36-43,47 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/02/04 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 36-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Okutsu et al. (USP 6433623).

As to claims 1 and 36, Okutsu et al. discloses in figure 1 a level shift circuit comprising : a capacitor (C1); a charge control circuit (P16 and G14) connected to the capacitor for providing a voltage of a high potential power supply (Vcc) to the capacitor and controlling charging of the capacitor; and a limiting circuit (P15) connected to the high potential power supply and the charge control circuit for stopping the voltage provided to the capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor, wherein the limiting circuit limits the voltage provided to the

capacitor when boosting of an output signal (signal at node 9) of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started. As further called in for claim 36, figure 1 shows the charge control circuit comprises a first transistor (P16), and the limiting circuit comprises a second transistor (P15). *As seen in figure 1, when voltage at line T1 is high, the output of G14 is low, thereby turnoff transistor P15. As the same time, transistor P17 is on, thereby connects the gate and drain of transistor P16 together. However, transistor P16 will not turn off until its source drain potential is less than its threshold voltage. Therefore, transistor P16 turns off after transistor P15 turns off.*

As to claim 37, figure 1 shows the second transistor is transistor is turned off by a control signal generated on the basis of an input signal (output of G9).

As to claim 38, figure 1 shows the second transistor is turned off when stepping up a voltage of an input signal (inherent).

As to claim 39, figure 1 shows the second transistor limits a flow of current from the capacitor to the high potential power supply.

As to claim 40, figure 1 shows the limiting circuit includes a transistor (P12).

As to claim 41, figure 1 shows transistor P12 is turned off when limiting the voltage provided to the capacitor.

As to claim 42, figure 1 shows the transistor (P12) limits a flow of current from the capacitor to the high potential power supply.

Claim 43 recites similar limitations of claims 1 and 36. Therefore, it is rejected with the same reasons.

As to claim 47, figure 1 shows the charge control circuit includes an inverter (G14) provided between the high potential power supply and a low potential power supply.

3. Claim 48 is rejected under 35 U.S.C. 102(e) as being anticipated by Hideo (JP 10-144080) (newly cited).

Hideo discloses in figure 3 a level shift circuit comprising: a capacitor (Qa); a charge control circuit (Tr4) connected to the capacitor for providing a voltage of a high potential power supply (Vcc) to the capacitor in accordance with a first control signal (V4) and controlling charging of the capacitor; and a limiting circuit (Tr3) connected to the high potential power supply and the charge control circuit for stopping the voltage provided to the capacitor from the high potential power supply in accordance with a second control signal (output of 32) that changes faster, based on an input signal, than the first control signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (USP 6060930) in view of Tomobe et al. (USP 6198334).

Choi discloses in figure 1 a circuit comprising a capacitor (MN1) and a charge control circuit (IN1). Choi fails to show the charge control circuit having first and second transistors for charging the capacitor. However, Tomobe et al.'s figure 3 shows an inverter circuit with an advantage of eliminating noise. Therefore, it would have been obvious to one having ordinary

skill in the art to use Tomobe et al.'s inverter for Choi's inverter for the purpose of eliminating noise. Thus, the modified Choi's figure 1 further shows: a charge control circuit (Tomobe et al.'s P2) connected to the capacitor for providing a voltage of a high potential power supply (Vcc) to the capacitor in accordance with a first control signal (output of the delay circuit 1) and controlling charging of the capacitor; and a limiting circuit (Tomobe et al.'s P1) connected to the high potential power supply and the charge control circuit for stopping the voltage provided to the capacitor from the high potential power supply in accordance with a second control signal that changes faster, based on an input signal, than the first control signal.

Allowable Subject Matter

6. Claims 2-10 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

May 17, 2004